DMX512 testing—Still room for improvement

BY **BOB GODDARD**

DMX512 DATES BACK TO 1986. Its adoption as the dominant protocol for digital lighting data transmission has been pervasive. The first commercially produced DMX512 tester came to market 25 years ago. One might think that there isn't much left to be said about testing DMX512.

One would be mistaken.

Recently, DMX512 has found a growing acceptance as the control protocol for multi-color LED luminaires. This has brought many new players to the DMX community, underscoring the need for rigorous compliance and acceptance testing. There is one error condition that a surprising number of DMX512 receivers fail to handle properly. I recently found that I needed to test a receiver's DMX performance while running tests on its RDM compliance. The RDM compliance was spot on; the DMX performance was lacking.

DMX512 has next to no error detection. DMX512 does not use a check sum. It does not check parity. Packets are of unknown length. Determining when a DMX packet has ended can be done any of three ways: You see the Break starting the next packet, there has been a one second interval with no new slots, or you have received 512 slots of data.

Framing errors should be rejected

One limit that DMX512 does place from *ANSI E1.11 – 2008 (R2013) Entertainment Technology USITT DMX512-A Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories* is:

> **"9.1 Rejection of Improperly framed slots**
>
> A receiver shall check the first stop bit and should check the second stop bit of all received slots to determine if they have the correct value. If a missing stop bit is detected, the receiver shall discard the improperly framed slot data and all following slots in the packet."

The **Figure 1** DMX512 timing drawing from *E1.11* is shown in the accompanying line-drawing. DMX uses an 8-bit serial, asynchronous data transmission method. DMX512 sends data in packets made up of a sequence of framed slot data. The framing consists of one leading Start bit (#4 in the timing drawing) and two trailing Stop bits (#7 and #8 in the timing drawing). The beginning of the packet is marked by a Break (#1) and Mark After Break (#2). The Break is a low of at least 88 µs. The Break/MAB sequence signals the end of the last packet and the beginning of the new packet. It

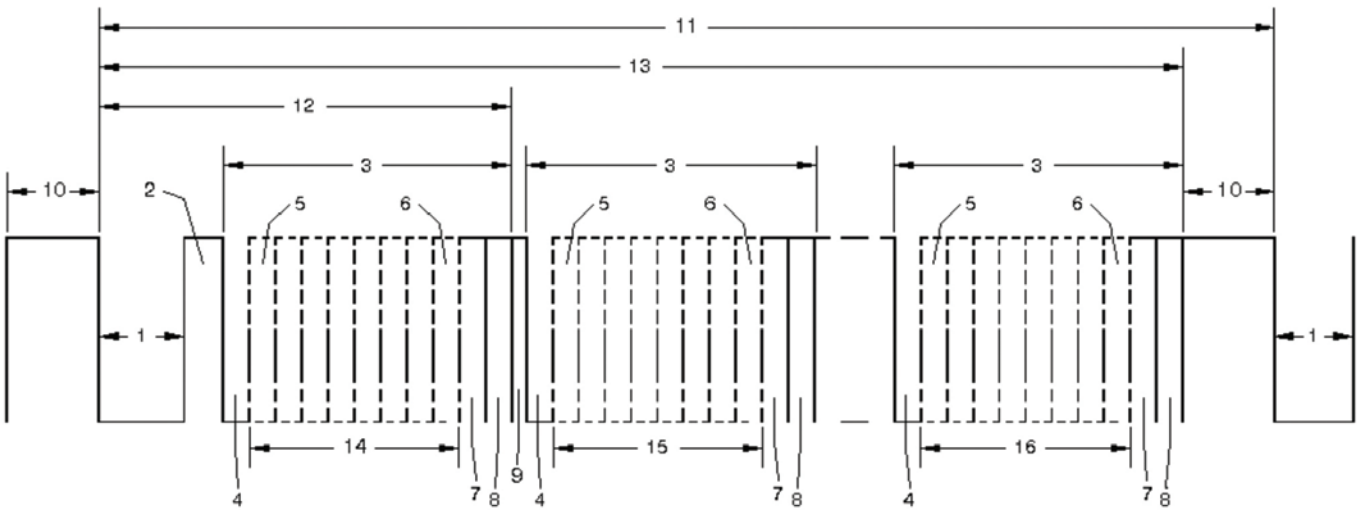

Figure 1 – DMX512 timing drawing

also resets the address counter.

A frame starts at the falling edge of the Start bit. The receiver re-samples the line 2 µs later. If the line is still low, the controller is sending a slot. The receiver then waits 4 µs and reads the value of the least significant bit (LSB). It waits another 4 µs and samples the next more significant bit. It repeats this wait and sample routine six more times for data and two times to get the Stop bits.

DMX512 has found a growing acceptance as the control protocol for multi-color LED luminaires.

If electronic noise corrupts only one bit, and if it isn't one of the stop bits, we have no way to detect it. The good news is that the corruption should only affect one slot. However, multiple bits or multiple frames are often damaged. A receiver reads the line 40 µs after the falling edge of the Start bit. It should be high; if not, the first Stop bit is missing. If 4 µs later the line is still low, the second Stop bit is missing as well. When the line goes high and then low, the receiver will assume that a new frame has started.

According to *ANSI E1.11* section 9.1, if either of the Stop bits is low, then data from that frame should be discarded, and all data until the next Break/MAB sequence should also be discarded. The receiver has no way of knowing how many frames were damaged and can no longer reliably count frames. The address counter may be pointing to the wrong location. If the address counter misses a count, the slot mapping will corrupt. All slot data may shift. This is one of the ugliest errors you will ever see! Red becomes green, all the movers hiccup, your 2Ks' data has suddenly been sent to the 12Ks.

It seems to be a no-brainer that testing to detect this issue is in everyone's interest, and the results should be simple to interpret.

Testing for framing errors

The following test clearly shows how a DMX receiver handles packets with a framing error.

A test controller sends a test packet repetitively. At some triggering event, either manual or automated, it sends a packet that has 1 frame (slot) with the first Stop bit set low. The data in that frame is changed by complementing the 8th bit, changing the value of that slot by +/-80 hex. The rest of the frames in that packet are sent with the proper Stop bits, but they too have the value of the 8th bit complemented. The packet with errors is sent 10 times. Then the controller returns to normal operation.

If the device under test discards the frame with the error and discards all following frames, no visual change should be seen. A DMX512 receiver is required to work with update rates as low as one per second—so, the receiver should hold the last good packet. If you see major flashing, then the receiver failed.

Framing in pictures

The bottom trace shows two full framed slots of a normal packet and the beginning of a third. On the left is the falling edge of the Start bit of the first slot. The data in the first slot is 00h. The data line stays low for 36 µs. The Start bit and each of the 8 bits lasts 4 µs.

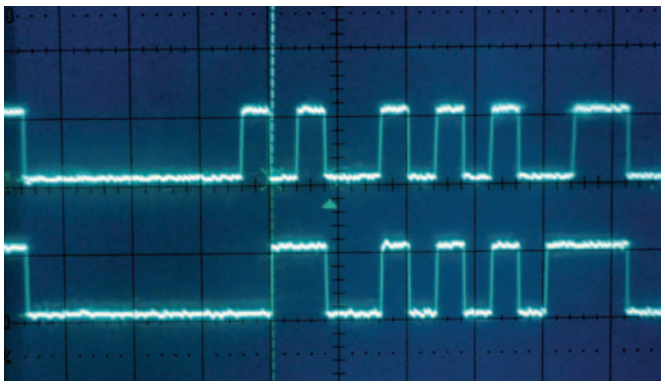

Figure 2 – Oscilloscope images showing normal and malformed frames. Horizontal = 10 µs/division; Vertical = 5 V/division

At the end of the 8th data bit the line goes high. It stays high for 8 µs (the length of time for two Stop bits). (The vertical cursor is at the beginning of the first Stop bit.) After the Stop bits the line goes low for the Start bit of the next frame. The data in the second slot is AAh sent as 01010101. The 8th data bit and the two Stop bits make up the 12 µs high before the line goes low for the beginning of a third slot (extreme right side).

If electronic noise corrupts only one bit, and if it isn't one of the Stop bits, we have no way to detect it.

The top trace shows the same two framed slots. However, the first Stop bit of the first frame is set low. Note that the low to high transition of the Stop bit should align with the cursor, but does not.

The data in the first slot is now 80h because we have complemented the 8th data bit (the high bit before the cursor). The second slot now has a value of 2Ah because we have complemented its 8th bit as well.

DMX is robust, but . . .

The DMX512 transmission system is usually robust and runs with a very low error rate. Since it is a streaming protocol, errors are quickly over-written and often invisible. But not always. Problems do happen with electromagnetic interference on the transmission line. We have all spent far too long (often late at night) chasing gremlins. Since an error attributable to framing can be spectacular, it would be nice to know that the equipment you are about to install rejects packets with corrupted framing.

. . . an error attributable to framing can be spectacular . . .

Our upcoming software releases will include this test. While we have not seen a similar test supported by other production testers, we do not claim that ours is unique. We hope a similar test becomes part of other test suites. ■

Robert Goddard heads Goddard Design Co. He is the architect of the DMXter family of DMX512 and RDM testers and verifiers. Over the years, he has designed and built numerous entertainment and architectural lighting control systems. Bob is a named inventor on 12 US and several foreign patents. He also offers consulting services and can be reached at rmg@goddarddesign.com.